# Abstracts

## Device and circuit-level modeling using neural networks with faster training based on network sparsity

Recently, circuit analysis and optimization featuring neural-network models have been proposed, reducing the computational time during optimization while keeping the accuracy of physics-based models. We present a novel approach for fast training of such neural-network models based on the sparse matrix concept. The new training technique does not require any structure change in neural networks, but makes use of the inherent nature of neural networks that for each pattern some neuron activations are close to zero, and hence, have no effect on network outputs and weights update. Much of the computation effort is saved over standard training techniques, while achieving the same accuracy. FET device and VLSI interconnect modeling examples verified the proposed technique.

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